

## TEAC

## **SERVICE MANUAL**

# PD-H300C

**Compact Disc Player** 

#### NOTES

- PC boards shown are viewed from parts side.
- The parts with no reference number or no parts number in the exploded views are not supplied.
- As regards the resistors and capacitors, refer to the circuit diagrams contained in this manual.
- Parts marked with this sign are safety critical components.

They must be replaced with identical components- refer to the appropriate parts list and ensure exact replacement.

Parts of [ ] mark can be used only with the version designated

[DM]: JAPAN [T/C]: U.S.A, CANADA [EUR]: EUROPE [UK]: UK

### **CONTENTS**

SPECIFICATIONS
MEASUREMENT AND ADJUSTMENT METHODS
IC PIN FUNCTION
WIRING DIAGRAM
BLOCK DIAGRAM
SCHEMATIC DIAGRAM
PRINTED CIRCUIT BOARDS
EXPLODED VIEW
ELECTRICAL PARTS LIST

## **Specifications**

Laser System : 3-beam laser

Digital Filter : 8-times oversampling Frequency Response : 20-20,000Hz( $\pm 2$ dB)

Error Correction Method:

Cross Interleave Reed-Solomon code

S/N Ratio : More than 100dB

(IHF "A" Filter used)

T.H.D : Less than 0.02% (1KHz)

Output Voltage : 2V RMS

Power requirements: 230V, 50Hz [EUR]

100V, 50Hz [DM]

Power Consumption: 9W [EUR]

8W [DM]

Dimensions (W×H×D):  $285 \times 131 \times 292$ mm

Weight : 3.9Kg

**Standard accessories** 

Remote control cord......1
Signal cord......1

\* Improvements may result in specification or

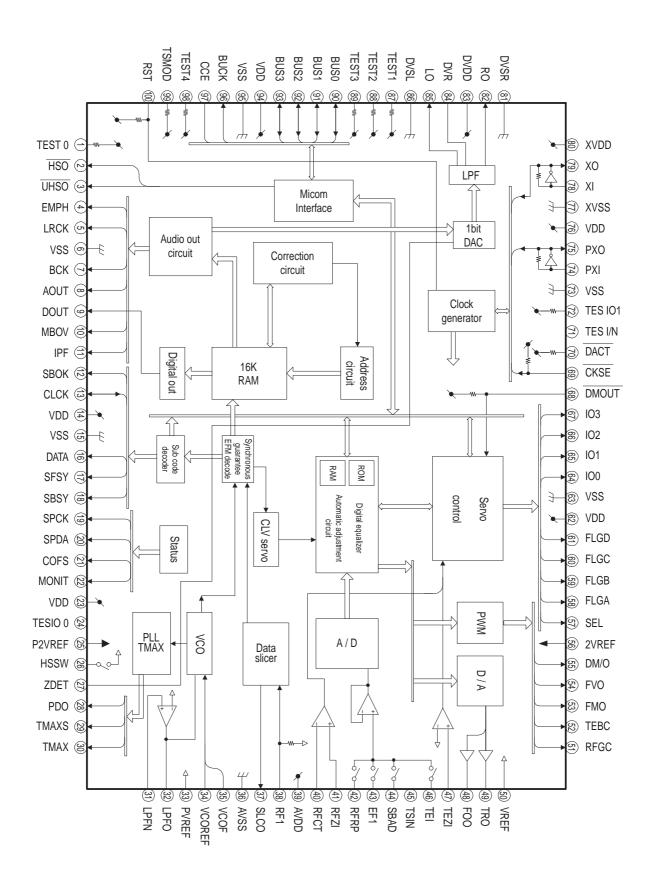
feature changes without notice.

## TC9432AF/ TC9462AF (Digital Signal Processor)

PIN No.	NAME	I/O	FUNCTIONAL DESCRIPTION	REMARKS
1	TEST0	-	Test mode terminal. Normally, keep at open.	With pull-up resistor.
			Playback speed mode flag output terminal.	
2	HSO	0	UHSO HSO PLAYBACK SPEED H H Normal	-
3	UHSO	0	H         L         2 times           L         H         4 times           L         L         -	
4	EMPH	0	Subcode Q data emphasis flag output terminal. Emphasis ON at "H" level and OFF at "L" level. The output polarity can invert by command.	-
5	LRCK	0	Channel clock output terminal. (44.1 kHz) L-ch at "L" level and R-ch at "H" level. The output polarity can invert by command.	-
6	Vss	-	Digital GND terminal.	-
7	BCK	0	Bit clock output terminal. (1.4112 MHz)	-
8	AOUT	0	Audio data output terminal.	-
9	DOUT	0	Digital data output terminal.	-
10	MBOV	0	Buffer memory over signal output terminal.  Over at "H" level.	-
11	IPF	0	Correction flag output terminal. At "H" level, AOUT output is made to correction impossibility by C2 correction processing.	-
12	SBOK	0	Subcode Q data CRCC check adjusting result output terminal. The adjusting result is OK at "H" level.	-
13	CLCK	I/O	Subcode P~W data readout clock input/output terminal. This terminal can select by command bit.	-
14	VDD	-	Digital power supply voltage terminal.	-
15	Vss	-	Digital GND terminal.	-
16	DATA	0	Subcode P~W data output terminal.	-
17	SFSY	0	Playback frame sync signal output terminal.	-
18	SBSY	0	Subcode block sync signal output terminal.	-
19	SPCK	0	Processor status signal readout clock output terminal.	-
20	SPDA	0	Processor status signal output terminal.	-
21	COFS	0	Correction frame clock output terminal. (7.35 kHz)	-
22	MONIT	0	Internal signal (DSP internal flag and PLL clock) output terminal. Selected by command.	-
23	VDD	-	Digital power supply voltage terminal.	-
24	TESIO0	I	Test input/output terminal. Normally, keep at "L" level.	-
25	P2Vref	-	PLL double reference voltage supply terminal.	-
26	HSSW	0	2/4 times speed at "VREF" voltage.	2-state output (PVREF,HiZ)
27	ZDET	0	1 bit DA converter zero detect flag output terminal.	-
28	PDO	0	Phase difference signal output terminal of EFM signal and PLCK signal.	3-state output (P2VREF,PVREF,VSS)
29	TMAXS	0	TMAX detection result output terminal. Selected by command bit (TMPS).	-
30	TMAX	0	TMAX detection result output terminal. Selected by command bit (TMPS).  DIFFERENCE RESULT TMAX OUTPUT  Longer than fixed ferq. "P2VREF"  Shorter than fixed freq. "Vss"  Within the fixed freq. "HiZ"	3-state output (P2VREF,HiZ,VSS)

PIN No.	NAME	I/O	FUNCTIONAL DESCRIPTION	REMARKS
31	LPFN	ı	LPF amplifier inverting input terminal for PLL.	Analog input.
32	LPFO	0	LPF amplifier output terminal for PLL.	Analog output.
33	PVref	_	PLL reference voltage supply terminal.	-
34	VCOREF	I	VCO center frequency reference level terminal. Normally, keep at "PVREF" level.	-
35	VCOF	0	VCO filter terminal.	Analog output.
36	AVss	-	Analog GND terminal.	-
37	SLCO	0	Data slice level output terminal.	Analog output.
38	RFI	ı	RF signal input terminal.	Analog input (Zin : selected by command)
39	AVDD	-	Analog power supply voltage terminal.	-
40	RFCT	ı	RFRP signal center level input terminal.	Analog input (Zin : 50kΩ)
41	RFZI	ı	RFRP zero cross input terminal.	Analog input.
42	RFRP	ı	RF ripple signal input terminal.	Analog input.
43	FEI	ı	Focus error signal input terminal.	Analog input.
44	SBAD	I	Sub-beam adder signal input terminal.	Analog input.
45	TSIN	ı	Test input terminal. Normally, keep at "VREF" level.	Analog input.
46	TEI	ı	Tracking error signal input terminal. Track in at tracking servo on.	Analog input.
47	TEZI	ı	Trcaking error zero cross input terminal.	Analog input (Zin : 10k Ω)
48	FOO	0	Focus servo equalizer output terminal.	Analog output (2VREF~AVSS)
49	TRO	0	Tracking servo equalizer output terminal.	
50	VREF	-	Analog reference voltage supply terminal.	
51	RFGC	0	RF amplitude adjustment control signal output terminal.	-
52	TEBC	0	Tracking balance control signal output terminal.	3-state PWM signal output.
53	TEBC	0	Feed equalizer output terminal.	(2VREF, VREF, VSS)
54	TEBC	0	Speed error signal or feed search equalizer output terminal.	(PWM carrier = 88.2 kHz)
55	DMO	0	Disk equalizer output terminal. (PWM carrier = 88.2 kHz for DSP, Synchronize to PXO)	3-state PWM signal output.(2VREF, VREF, VSS)
56	2VREF	_	Analog double reference voltage supply terminal.	_
57	SEL	0	APC circuit ON/OFF indication signal output terminal. At the laser on time, UHF = L at "HiZ" level and UHF = H at "H" level.	-
58	FLGA	0	External flag output terminal for internal signal. Can select signal from TEZC, FOON, FOK and RFZC by command.	-
59	FLGB	0	External flag output terminal for internal signal. Can select signal from DECT, FOON, FMON and RFZC by command.	-
60	FLGC	0	External flag output terminal for internal signal. Can select signal from TRON, TRSR, FOK and SRCH by command.	-
61	FLGD	0	External flag output terminal for internal signal.  Can select signal from TRON, DMON, HYS and SHC by command.	-
62	Vdd	-	Digital power supply voltage terminal.	-
63	Vss	-	Digital GND terminal.	-
64	IO0		General I/O terminal. Can change over input port or	
65	IO1	1	output port by command. At the input mode time can	
66	IO2	I/O	readout a state of terminal (H/L) by read command. At the output mode time can control a state of terminal	-
67	IO3		(H/L/HiZ) by command.	

PIN No.	NAME	I/O	FUNCTIONAL DESCRIPTION	REMARKS
68	DMOUT	I	This terminal controls IO0~IO3 terminal. At "L" level time, IO0, 1 out feed equalizer signal of 2-state PWM. IO2, 3 out disk equalizer signal of 2-state PWM.	With pull-up resistor.
69	CKSE	I	Normally, keep at open.	With pull-up resistor.
70	DACT	I	DAC test mode terminal. Normally, keep at open.	With pull-up resistor.
71	TESIN	I	Test input terminal. Normally, keep at "L" level.	Analog input.
72	TESIO1	I	Test input/output terminal. Normally, keep at "L" level.	Analog input.
73	Vss	-	Digital GND terminal.	-
74	PXI	I	Crystal oscillator connecting input terminal for DSP. Normally, keep at "L" level.	_
75	PXO	0	Crystal oscillator connecting output terminal for DSP.	
76	VDD	-	Digital power supply voltage terminal.	-
77	XVss	-	Oscillator GND terminal for system clock.	-
78	ΧI	I	Crystal oscillator connecting input terminal for system clock.	-
79	XO	0	Crystal oscillator connecting output terminal for system clock.	-
80	XVDD	-	Oscillator power supply voltage terminal for system clock.	-
81	DVsR	-	Analog GND terminal for DA converter. (R-ch)	-
82	RO	0	R channel data forward output terminal.	-
83	DVdd	-	Analog supply voltage terminal for DA converter.	-
84	DVR	-	Reference voltage terminal for DA converter.	-
85	LO	0	L channel data forward output terminal.	-
86	DVsL	-	Analog GND terminal for DA converter. (L-ch)	-
87	TEST1	- 1	Test mode terminal. Normal, keep at open.	With pull-up resistor.
88	TEST2	I	Test mode terminal. Normal, keep at open.	With pull-up resistor.
89	TEST3	I	Test mode terminal. Normal, keep at open.	With pull-up resistor.
90	BUS0	I/O		
91	BUS1	I/O	Micom interface data input/output terminal.	Schmit input.
92	BUS2	I/O		With pull-up resistor.
93	BUS3	I/O		
94	VDD	-	Digital Ppower supply voltage terminal.	-
95	Vss	-	Digital GND terminal.	-
96	BUCK	I	Micom interface clock input terminal.	Schmit input.
97	CCE	I	Command and data sending/receiving chip enable signal input terminal. The bus line becomes active at "L" level.	Schmit input.
98	TEST4	I	Test mode terminal. Normal, keep at open.	With pull-up resistor.
99	TSMOD	I	Local test mode selection terminal.	With pull-up resistor.
100	RST	- 1	Reset signal input terminal. Reset at "L" level.	With pull-up resistor.

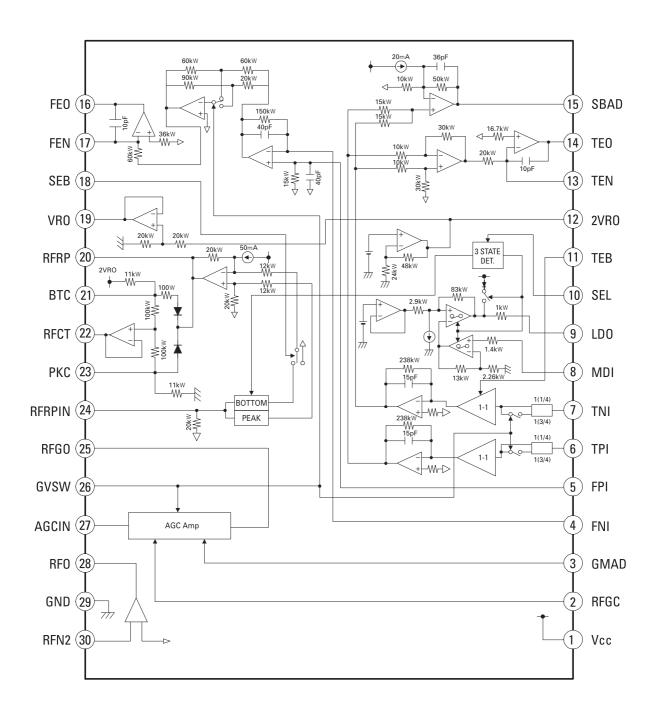


#### TA2150FN

PIN No.	SYMBOL	I/O	FUNCTION DESCRIPTION	REMARKS
1	VCC	-	Power supply input terminal.	-
2	RFGC	I	RF amplitude adjustment control signal input terminal.  Controlled by 3-PWM signals.  (PWM carrier = 88.2kHz)	3 signals input. (2VRO, VRo, GND)
3	GMAD	I	Open loop gain adjustment terminal for AGC amp.	(Note 1)
4	FNI	I	Main beam I-V amp input terminal.	Connected to pin diode output B + D (through resistor)
5	FPI	I	Main beam I-V amp input terminal.	Connected to pin diode output A + C (through resistor)
6	TPI	I	Sub beam I-V amp input terminal.	Connected to pin diode output F.
7	TNI	I	Sub beam I-V amp input terminal.	Connected to pin diode output E.
8	MDI	I	Monitor photo diode amp input terminal.	Connected to pin monitor photo diode.
9	LDO	0	Laser diode amp input terminal.	Connected to laser diode control circuit.
10	SEL	I	Laser diode control signal input terminal and APC circuit ON/OFF control signal terminal.  SEL APC LEVEL CIRCUIT LDO DETECT FREQUENCY  GND OFF Connected to Vcc through resister (1 k \Omega) Low  Hiz ON Control signal output Low  Vcc ON Control signal output High	3 signals input. (Vcc, Hiz, GND)
11	TEB	I	Tracking error balance adjustment signal input terminal. Controlled by 3-PWM signal.  (PWM carrier = 88.2 kHz)	3 signals input (2VRO, VRO, GND)
12	2VRO	0	Reference voltage (2VRO) output terminal. 2VRO = 4.2 V when Vcc = 5 V	-
13	TEN	I	TE amp negative input terminal.	Connected to TEO through feedback resistor.
14	TEO	0	TE error signal output terminal.	-
15	SBAD	0	Sub beam adder signal output terminal.	-
16	FEO	0	Focus error signal output terminal.	-
17	FEN	I	FE amp negative input terminal.	Connected to FEO through feedback resistor.
18	SEB	I	RFRP output circuit suitching terminal.  SEB LEVEL BOTTON PEAK DETECTION GND GND GND GND GND GND GND GND	Low (GND) is for normal use.

## TA2150FN

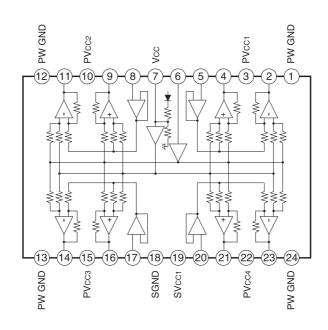
PIN No.	SYMBOL	I/O	FUNCTION DESCRIPTION	REMARKS
19	VRO	0	Reference signal (VRO) output terminal. VRO = 2.1 V when Vcc = 5 V	-
20	RFRP	0	Track count signal output terminal.	-
21	BTC	I	Time constant adjustment terminal for bottom detection.	Adjusted by capacitance.
22	RFCT	0	RFRP signal center level output terminal.	-
23	PKC	I	Time constant adjustment terminal for peak detection.	Adjusted by capacitance.
24	RFRPIN	Ι	Input terminal for track count signal output amp.	-
25	RFGO	0	Output terminal for RF signal amplitude adjustment amp.	-
26	GVSW	I	Amp (AGC, FE, TE) gain switching terminal.  GVSW MODE  GND CD-RW  Hiz Normal  Vcc Normal	Low (GND) is for 5 times gain.
27	AGCIN	I	Input terminal for RF signal amplitude adjustment amp.	Connected to RFO through capacitance.
28	RFO	0	Output terminal RF signal amp.	-
29	GND	-	Ground terminal.	-
30	RFN2	I	input terminal for RF signal amp.	Connected to pin-diode output A + B + C + D (through resistor).



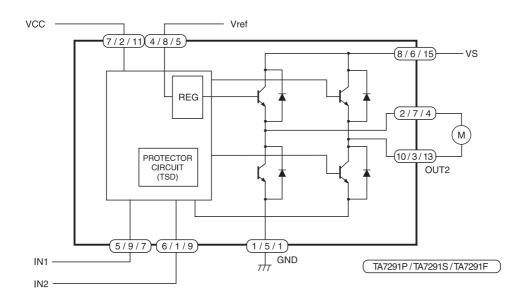
## **TA2092N (POWER DRIVER)**

PIN No.	NAME	DESCRIPTION
		Power GND
1	PW GND	Connected to substrate.
		① , ⑫ , ⑬ , ❷ pin are connected inside.
2	OUT (-) 1	Inverted output for CH1
0	DV/	Supply terminal of output stage for CH1
3	PV <sub>CC1</sub>	Supply terminal of output stage are not connected to other channel terminal.
4	OUT (+) 1	Non-inverted output for CH1
5	VIN1	Input for CH1. Not biased inside
		Input reference voltage
6	Vri	Under condition of VRI ≤ 1.8V, internal bias circuit is shut off.
		No signal input condition : VRI = VIN
7	Vcı	Output reference voltage. Vout = VcI = (Vcc-VF)/2
8	VIN2	Input for CH2
9	OUT (+) 2	Non-inverted output for CH2
10	PVcc2	Supply terminal of output stage for CH2
11	OUT (-) 2	Inverted output for CH2
12	PW GND	Power GND
13	PW GND	Power GND
14	OUT (-) 3	Inverted output for CH3
15	РУссз	Supply terminal of output stage for CH3
16	OUT (+) 3	Non-inverted output for CH3
17	VIN3	Input for CH3
18	S GND	Supply terminal of small signal GND
19	S Vcc	Small signal GND
20	VIN4	Input for CH4
21	OUT (+) 4	Non-invered output for CH4
22	Pvcc4	Supply terminal of output stage for CH4
23	OUT (-) 4	Inverted output for CH4
24	PW GND	Power GND

#### **BLOCK DIAGRAM**



## **TA7291S (Bridge Driver)**

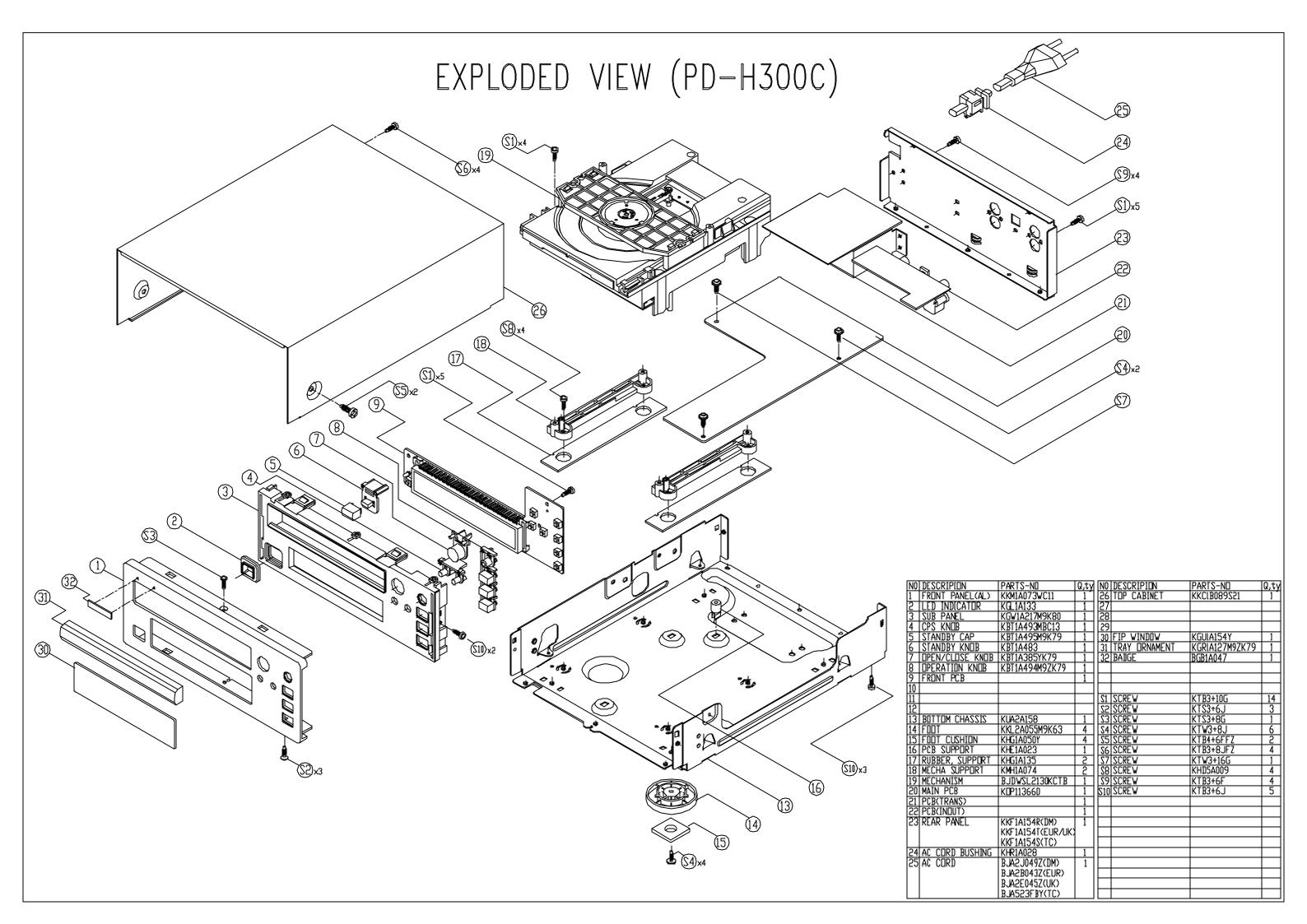


PIN	No.	CVA	VIBOL FUNCTIONAL DESCRIPTION
Р	S	311	VIBOL FUNCTIONAL DESCRIPTION
7	2	Vcc Supply voltage terminal for Logic	
8	6	Vs	Supply voltage terminal for motor drive
4	8	Vref Supply voltage terminal for control	
1	5	GND GND terminal	
5	9	IN1 Input terminal	
6	1	IN2	Input terminal
2	7	OUT1 Output terminal	
10	3	OUT2	Output terminal

P Type: PIN ③, ⑨: NCS Type: PIN 4: NC

• F Type : PIN 2), 3), 6), 8), 10), 12), 14), and 16 : NC

• For F Type, We recommend FIN to be connected to the GND.



#### **EXPLODED VIEW LIST**

REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
1	9A08789800	PANEL, FRONT(AL)	KKM1A073WC11
2	9A06863300	INDICATOR, STAND BY	KGL1A133
3	9A07436000	PANEL, SUB	KGW1A217M9K80
4	9A06868300	KNOB, CPS	KBT1A493MBC13
5	9A07287200	CAP, STANBY	KBT1A495M9K79
6	9A06862500	KNOB, STAND BY	KBT1A483
7	9A07431800	KNOB, TACT (OPEN/CLOSE)	KBT1A385YK79
8	9A07287100	KNOB, OPERATION	KBT1A494M9ZK79
9	9A08790100	CD SUB PCB ASS'Y	K0P11368B
13	9A06871600	CHASSIS, BOTTOM	KUA2A158
14	9A06864400	FOOT	KKL2A055M9K63
15	9A05837300	FOOT CUSHION	KHG1A050Y
16	9A06229100	MOUNT, PCB	KHE1A023
17	9A06241400	RUBBER, SUPPORT	KHG1A135
18	9A06870600	SUPPORT, MECHA	KMH1A074
19	9A08788100	CD MECHANISM ASS'Y	BJDWSL2130KCTB
L	9A08788800	CD PICK-UP ASS'Y	HJDKCTB1H
20	9A08790000	CD MAIN PCB ASS'Y	K0P11366DEUR
21	9A08790000	CD MAIN PCB ASS'Y	KOP11366DEUR
22	9A08790000	CD MAIN PCB ASS'Y	K0P11366DEUR
23	9 <b>A</b> 08789700	PANEL, REAR	KKF1A154T
24	♠ 9A06754900	BUSHING, AC CORD	KHR1A028
25	♠ 9A08152100	POWER CORD, 2.5A 250V	BJA2B043Z
26	9A06870100	CABINET, TOP	KKC1B089S21
30	9A06240500	WINDOW	KGU1A154Y
31	9A07435900	ORNAMENT, TRAY	KGR1A127M9ZK79
32	9A06224200	BADGE, TEAC	BGB1A047
F101	↑ 9A06868100	FUSE	KBA2C0315TLE

#### **INCLUDED ACCESSORIES**

REF.NO.	PARTS NO.	DESCRIPTION	REMARKS
	9A08524200	OWNER'S MNL, EUR	KQX1A620Z
	9A05935900	CORD, PIN	KJS4M014Y
	9A05936000	CORD, PIN	KJS4N001Y

#### **CD MAIN PCB ASSY**

<b>OD</b> 1017 (11	• • •	<i>7</i>	
REF.NO.		PARTS NO.	DESCRIPTION
		9A08790000	CD MAIN PCB ASS'Y
		9A08790600	CD MAIN PCB
		9A05961500	PLATE, EARTH
		9A05328200	HOLDER, FUSE
		9A05333500	HEAT SINK
		9A08038100	RING, FERRITE
BD01		9A07050600	BEAD, CORE
C208	$\triangle$	9A06764800	C, ELECT 100UF/50V
C209	$\triangle$	9A05976300	C, ELECT 2200UF/35V
C213, 214	$\triangle$	9A06226700	C, ELECT 1000UF/25V
C223	$\triangle$	9A06764900	C, ELECT 100UF/35V
CN01		9A08220300	WAFER, CARD CABLE
CN02		9A05329700	WAFER, MOLEX53014-0610
CN03		9A05356400	WAFER, MOLEX53014-0510
CN04		9A08789600	WAFER, CARD CABLE
21125			W.F.F. 0 0151 F
CN05		9A08789500	WAFER, C. CABLE
CN06		9A05331000	WAFER, MOLEX 53014-1210
CN08		9A06674400	WAFER
CN09	Δ	9A05967800	WAFER
D102, 103	A	9A05194600	DIODE, 1N4003SRT
D104	$\triangle$	9A05194700	DIODE, 1N4003ST
D105	$\overline{\wedge}$	9A06765100	DIODE, ZENER MTZJ27BT
D106		9A06236200	DIODE, ZENER MTZJ6.2BT
D110,111		9A01390500	DIODE, 1N4148MT
D112		9A05194600	DIODE, 1N4003SRT
D500-502		9A01390500	DIODE, 1N4148MT
D503		9A06236200	DIODE, ZENER MTZJ6.2BT
D504-509	$\triangle$	9A05194600	DIODE, 1N4003SRT
IC01		9A08788500	IC, TA2150FN
IC02		9A08788700	IC, TC9462F
IC03		9A08788400	IC, TA2092N
1C04		9A08788600	IC, TA7291S
IC05		9A06786000	IC, TMP87PM78F
IC09, 10		9A07343300	IC, NJM2068MD-TE1
IC11	$\triangle$	9A08788200	IC, NJM7809FA
	_		, , , , , , , , , , , , , , , , , , , ,
IC12	$\triangle$	9A08788300	IC, NJM7909FA
IC14,15	$\triangle$	9A05341500	IC, KA7805-ABTU
IC21	$\triangle$	9A08790800	IC, KA78R08
JK50		9A06869700	JACK, BOARD
JK51		9A06239100	MODULE, OPTICAL
IVEO		0406960900	IACK IN (OUT (D /D C)
JK52		9A06869800	JACK, IN/OUT (B/B, G)
L102, 103		9A07330400	COIL, AXAIL 10HH K
L104		9A05356900	COIL, AXAIL 10UH K
0104, 107		9A08791000	TR, KRA107M TR, KRC107M
0108		9A08791100	In, KNCIU/M
0111		9A05196700	TR, KSA916-Y-SHTA
0112, 113		9A05197400	TR, KTC3203YT
0114		9A03745100	TR, KSA1175-YTA
0115		9A03745000	TR, KSC2785-YTA
Q116		9A05895900	TR, KTA1266YT

#### **CD MAIN PCB ASSY**

REF.NO.		PARTS NO.	DESCRIPTION
<b>Q</b> 500,501		9A05197500	TR, KTD1302T
<b>Q</b> 502		9A08791000	TR, KRA107M
<b>Q</b> 503		9A08791100	TR, KRC107M
<b>Q</b> 504		9A03745100	TR, KSA1175-YTA
T101	$\triangle$	9A08789900	TRANS, POWER
X101		9A05193100	CRYSTAL
X102		9A05193000	CRYSTAL

#### **CD SUB PCB ASSY**

REF. NO.	PARTS NO.	DESCRIPTION	
	9A08790100	CD SUB PCB ASS'Y	
	9A08790700	CD FRONT PCB	
BK01	9A05961600	BRACKET, FLT	
BK02	9A07290100	SUPPORT, LED	
CN04	9A08789600	WAFER, CARD CABLE	
CN05	9 <b>A</b> 08789500	WAFER, C. CABLE	
D101	9A08131100	LED, YELLOW	
FIP1	9A07313300	F.I.P. SVA08MS14	
S101-108	9A06671200	SW, TACT EV021505R	

